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L5	845	703/14.ccls.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2005/09/12 15:28
L6	333	717/106.ccls.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2005/09/12 15:29
L7	459	717/140.ccls.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2005/09/12 15:29
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IEEE CNF	IEEE Conference Proceeding
IEE CNF	IEE Conference Proceeding
IEEE STD	IEEE Standard

1. **ModelMaker: a tool for rapid modeling from device descriptions**
   Cyre, W.R.; Gunawan, A.;
   Verilog HDL Conference and VHDL International Users Forum, 1998. IVC/VIUF. Proceedings., 199
   16-19 March 1998 Page(s):138 - 142
   Digital Object Identifier 10.1109/IVC.1998.660692
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... Shyu Jong-Jy, Su Shih-Jae, **Yang Chun-Chih** and Lai Yo-Chuan, July 1997,"High-speed Reed-Solomon decoders," Fourth International Symposium on Communication ...
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[DOC] 論文題目：行政改革與政治控制的爭論
File Format: Microsoft Word 2000 - View as HTML
作者：楊鈞池(**Yang, Chun Chih**). 服務機構：國立高雄大學政治法律學系助理教授. (Assistant Professor; Department of Government and Law, National University of ...
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IEEE CNF	IEEE Conference Proceeding
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1. **Verification of VHDL designs using VAL**
Augustin, L.M.; Gennart, B.A.; Huh, Y.; Luckham, D.C.; Stanculescu, A.G.;
Design Automation Conference, 1988. Proceedings., 25th ACM/IEEE
12-15 June 1988 Page(s):48 - 53
Digital Object Identifier 10.1109/DAC.1988.14733
AbstractPlus | Full Text: PDF(476 KB) IEEE CNF

2. **Comment on "Event suppression by optimizing VHDL programs"**
Chang, K.C.;
Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on
Volume 18, Issue 9, Sept. 1999 Page(s):1400 - 1401
Digital Object Identifier 10.1109/43.784131
AbstractPlus | References | Full Text: PDF(32 KB) IEEE JNL

3. **On the use of VHDL as a multi-valued logic simulator**
Rozon, C.;
Multiple-Valued Logic, 1996. Proceedings., 26th International Symposium on
29-31 May 1996 Page(s):110 - 115
Digital Object Identifier 10.1109/ISMVL.1996.508345
AbstractPlus | Full Text: PDF(384 KB) IEEE CNF

4. **ModelMaker: a tool for rapid modeling from device descriptions**
Cyre, W.R.; Gunawan, A.;
Verilog HDL Conference and VHDL International Users Forum, 1998. IVC/VIUF. Proceedings., 199
16-19 March 1998 Page(s):138 - 142
Digital Object Identifier 10.1109/IVC.1998.660692
AbstractPlus | Full Text: PDF(104 KB) IEEE CNF

5. **Teaching design-oriented VHDL**
Pedroni, V.A.;
Microelectronic Systems Education, 2003. Proceedings. 2003 IEEE International Conference on
1-2 June 2003 Page(s):6 - 7
AbstractPlus | Full Text: PDF(352 KB) IEEE CNF

6. **Storage mechanism for VHDL intermediate form**
Poterie, B.;
Design Automation Conference, 1990. EDAC. Proceedings of the European

12-15 March 1990 Page(s):506 - 510
Digital Object Identifier 10.1109/EDAC.1990.136700

AbstractPlus | Full Text: PDF(332 KB) IEEE CNF

7. **The continuous-discrete interface - What does this really mean? Modelling and simulation is**
Brown, A.D.; Zwolinski, M.;
Circuits and Systems, 2003. ISCAS '03. Proceedings of the 2003 International Symposium on
Volume 3, 25-28 May 2003 Page(s):III-894 - III-897 vol.3

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1 High Level and Architectural Synthesis: Object oriented hardware synthesis and verification

T. Kuhn, T. Oppold, C. Schulz-Key, M. Winterholer, W. Rosenstiel, M. Edwards, Y. Kashai

September 2001 **Proceedings of the 14th international symposium on Systems synthesis**

Full text available: pdf(96.62 KB) Additional Information: full citation, abstract, references, citings, index terms

The synthesis of hardware from object oriented specifications is presented. Our approach utilizes the ***e*** language that has been proven to be highly efficient for the verification of hardware. The ***e*** language is similar to Java and provides additional constructs for specification and verification of hardware. We describe an automated design flow for the synthesis of object oriented descriptions that tightly integrates simulation based verification. The usability of our a ...

Keywords: high-level synthesis, object oriented hardware modeling, verification

2 A framework for object oriented hardware specification, verification, and synthesis

T. Kuhn, T. Oppold, M. Winterholer, W. Rosenstiel, Marc Edwards, Yaron Kashai

June 2001 **Proceedings of the 38th conference on Design automation**

Full text available: pdf(222.17 KB) Additional Information: full citation, abstract, references, citings, index terms

We describe two things. First, we present a uniform framework for object oriented specification and verification of hardware. For this purpose the object oriented language "e" is introduced along with a powerful run-time environment that enables the designer to perform the verification task. Second, we present an object oriented synthesis that enhances "e" and its dedicated run-time environment into a framework for specification, verification, and synthesis. The usab ...

Keywords: high-level synthesis, object oriented hardware modeling, verification

3 Polygon rendering on a stream architecture

John D. Owens, William J. Dally, Ujval J. Kapasi, Scott Rixner, Peter Mattson, Ben Mowery

August 2000 **Proceedings of the ACM SIGGRAPH/EUROGRAPHICS workshop on Graphics hardware**

Full text available: pdf(161.65 KB) Additional Information: full citation, abstract, references, citings, index terms

The use of a programmable stream architecture in polygon rendering provides a powerful mechanism to address the high performance needs of today's complex scenes as well as the need for flexibility and programmability in the polygon rendering pipeline. We describe how a polygon rendering pipeline maps into data streams and kernels that operate on streams, and how this mapping is used to implement the polgyon rendering pipeline on Imagine, a programmable stream processor. We compare our resul ...

Keywords: OpenGL, SIMD, graphics hardware, kernels, media processors, polygon rendering, stream architecture, stream processing, streams

4 Allowing for ILP in an embedded Java processor

Ramesh Radhakrishnan, Deependra Talla, Lizy Kurian John

May 2000 **ACM SIGARCH Computer Architecture News , Proceedings of the 27th annual international symposium on Computer architecture**, Volume 28 Issue 2

Full text available: pdf(293.70 KB) Additional Information: full citation, abstract, references, citings, index terms

Java processors are ideal for embedded and network computing applications such as Internet TV's, set-top boxes, smart phones, and other consumer electronics applications. In this paper, we investigate cost-effective microarchitectural techniques to exploit parallelism in Java bytecode streams. Firstly, we propose the use of a fill unit that stores decoded bytecodes into a decoded bytecode cache. This mechanism improves the fetch and decode bandwidth of Java processors by 2 to 3 time ...

5 Design of a SPDIF receiver using protocol compiler

Ulrich Holtmann, Peter Blinzer

May 1998 **Proceedings of the 35th annual conference on Design automation**

Full text available: pdf(348.72 KB) Publisher Site Additional Information: full citation, abstract, references, index terms

This paper describes the design of a receiver for the digital audio signal SPDIF used by CD-ROM players. The design was done with Protocol Compiler, a high-level synthesis tool for the design of structured data stream processing controllers. Compared to traditional RTL design, Protocol Compiler makes entry, debugging, and re-use easier. Design time was cut by factor 2 while the results in terms of area and delay are competitive.

Keywords: high-level synthesis, telecommunication

6 Instruction fetching: coping with code bloat

Richard Uhlig, David Nagle, Trevor Mudge, Stuart Sechrest, Joel Emer

May 1995 **ACM SIGARCH Computer Architecture News , Proceedings of the 22nd annual international symposium on Computer architecture**, Volume 23 Issue 2

Full text available: pdf(1.47 MB) Additional Information: full citation, abstract, references, citings, index terms

Previous research has shown that the SPEC benchmarks achieve low miss ratios in relatively small instruction caches. This paper presents evidence that current software-development practices produce applications that exhibit substantially higher instruction-cache miss ratios than do the SPEC benchmarks. To represent these trends, we have assembled a collection of applications, called the Instruction Benchmark Suite (IBS), that provides a better test of instruction-cache performance. We discuss th ...

7 A framework for fast hardware-software co-simulation

A. Hoffman, T. Kogel, H. Meyr

March 2001 **Proceedings of the conference on Design, automation and test in Europe**

Full text available: pdf(340.45 KB) Additional Information: full citation, references, citings, index terms

8 Spatial computation

Mihai Budiu, Girish Venkataramani, Tiberiu Chelcea, Seth Copen Goldstein

October 2004 **Proceedings of the 11th international conference on Architectural support for programming languages and operating systems**, Volume 32 , 39 , 38 Issue 5 , 11 , 5

Full text available: pdf(573.00 KB) Additional Information: full citation, abstract, references, index terms

This paper describes a computer architecture, *Spatial Computation* (SC), which is based on the translation of high-level language programs directly into hardware structures. SC program implementations are completely distributed, with no centralized control. SC circuits are optimized for *wires* at the expense of computation units.In this paper we investigate a particular implementation of SC: ASH (Application-Specific Hardware). Under the assumption that computation is cheaper than co ...

Keywords: application-specific hardware, dataflow machine, low-power, spatial computation

9 New tools and methods for future embedded SoC: Mapping a domain specific language to a platform FPGA

Chidamber Kulkarni, Gordon Brebner, Graham Schelle

June 2004 **Proceedings of the 41st annual conference on Design automation**

Full text available: pdf(165.71 KB) Additional Information: full citation, abstract, references, index terms

A domain specific language (DSL) enables designers to rapidly specify and implement systems for a particular domain, yielding designs that are easy to understand, reason about, re-use and maintain. However, there is usually a significant overhead in the required infrastructure to map such a DSL on to a programmable logic device. In this paper, we present a mapping of an existing DSL for the networking domain on to a platform FPGA by embedding the DSL into an existing language infrastructure. In ...

Keywords: domain specific language, network processing, platform FPGA

10 Formal verification in hardware design: a survey

Christoph Kern, Mark R. Greenstreet

April 1999 **ACM Transactions on Design Automation of Electronic Systems (TODAES)**, Volume 4 Issue 2

Full text available: pdf(411.53 KB) Additional Information: full citation, abstract, references, citings, index terms

In recent years, formal methods have emerged as an alternative approach to ensuring the quality and correctness of hardware designs, overcoming some of the limitations of traditional validation techniques such as simulation and testing. There are two main aspects to the application of formal methods in a design process: the formal framework used to specify desired properties of a design and the verification techniques and tools used to reason about the relationship between a spec ...

Keywords: case studies, formal methods, formal verification, hardware verification, language containment, model checking, survey, theorem proving

11 System-level power optimization: techniques and tools

Luca Benini, Giovanni de Micheli

April 2000 **ACM Transactions on Design Automation of Electronic Systems (TODAES)**, Volume 5 Issue 2

Full text available: pdf(385.22 KB) Additional Information: full citation, abstract, references, citings, index terms

This tutorial surveys design methods for energy-efficient system-level design. We consider electronic sytems consisting of a hardware platform and software layers. We consider the three major constituents of hardware that consume energy, namely computation, communication, and storage units, and we review methods of reducing their energy consumption. We also study models for analyzing the energy cost of software, and methods for energy-efficient software design and compilation. This survery ...

12 Architecture validation for processors

Richard C. Ho, C. Han Yang, Mark A. Horowitz, David L. Dill

May 1995 **ACM SIGARCH Computer Architecture News , Proceedings of the 22nd annual international symposium on Computer architecture**, Volume 23 Issue 2

Full text available: pdf(975.59 KB) Additional Information: full citation, abstract, references, citings, index terms

Modem, high performance microprocessors are extremely complex machines which require substantial validation effort to ensure functional correctness prior to tapeout. Generating the corner cases to test these designs is a mostly manual process, where completion is hard to judge. Experience shows that the errors that are caught late in the design, many post-silicon, are interactions between different components in very improbable corner case situations. In this paper we present a technique that ta ...

13 DMS®: Program Transformations for Practical Scalable Software Evolution

Ira D. Baxter, Christopher Pidgeon, Michael Mehlich

May 2004 **Proceedings of the 26th International Conference on Software Engineering**

Full text available: pdf(169.15 KB) Additional Information: full citation, abstract, citings

While a number of research systems have demonstratedthe potential value of program transformations, very few ofthese systems have made it into practice. The core technologyfor such systems is well understood; what remains isintegration and more importantly, the problem of handlingthe scale of the applications to be processed.This paper describes DMS, a practical, commercialprogram analysis and transformation system, and sketchesa variety of tasks to which it has been applied, from redocumentingt ...

14 Novel DFT, BIST and diagnosis techniques: Effective diagnostics through interval unloads in a BIST environment

Peter Wohl, John A. Waicukauski, Sanjay Patel, Greg Maston

June 2002 **Proceedings of the 39th conference on Design automation**

Full text available: pdf(155.82 KB) Additional Information: full citation, abstract, references, citings, index terms

Logic built-in self test (BIST) is increasingly being adopted to improve test quality and reduce test costs for rapidly growing designs. Compared to deterministic automated test pattern generation (ATPG), BIST presents inherent fault diagnostic challenges. Previous diagnostic techniques have been limited in their diagnosis resolution and/or require significant hardware overhead. This paper proposes an interval-based scan-unload method that ensures diagnosis resolution down to gate-level faults ...

Keywords: built-in self-test (BIST), fault diagnosis

15 Newlines and lexer states
Chris Clark
April 2000 **ACM SIGPLAN Notices**, Volume 35 Issue 4
Full text available: pdf(680.50 KB) Additional Information: full citation, index terms

16 Simulation vector generation from HDL descriptions for observability-enhanced statement coverage
Farzan Fallah, Pranav Ashar, Srinivas Devadas
June 1999 **Proceedings of the 36th ACM/IEEE conference on Design automation**
Full text available: pdf(151.12 KB) Additional Information: full citation, references, citings, index terms

17 Prophet/Critic Hybrid Branch Prediction
Ayose Falcon, Jared Stark, Alex Ramirez, Konrad Lai, Mateo Valero
March 2004 **ACM SIGARCH Computer Architecture News , Proceedings of the 31st annual international symposium on Computer architecture ISCA '04**, Volume 32 Issue 2
Full text available: pdf(214.72 KB) Additional Information: full citation, abstract, citings

This paper introduces the prophet/critic hybrid conditionalbranch predictor, which has two component predictorsthat play the role of either prophet or critic.Theprophet is a conventional predictor that uses branch historyto predict the direction of the current branch.Further accessesof the prophet yield predictions for the branches followingthe current one.Predictions for the current branchand the ones that follow are collectively known as thebranch's future.They are actually a prophecy, or pred ...

18 Preprototyping SIMD coprocessors using virtual machine emulation and trace compilation
Martin C. Herbordt, Owais Kidwai, Charles C. Weems
June 1997 **ACM SIGMETRICS Performance Evaluation Review , Proceedings of the 1997 ACM SIGMETRICS international conference on Measurement and modeling of computer systems**, Volume 25 Issue 1
Full text available: pdf(2.05 MB) Additional Information: full citation, abstract, references, index terms

The use of massively parallel SIMD array architectures is proliferating in the area of domain specific coprocessors. Even so, they have undergone few systematic empirical studies. The underlying problems include the size of the architecture space, the lack of portability of the test programs, and the inherent complexity of simulating up to hundreds of thousands of processing elements. We address the computational cost problem with a novel approach to trace-based simulation. Code is run on an abs ...

19 How to write Awk and Perl scripts to enable your EDA tools to work together
Robert C. Hutchins, Shankar Hemmady
June 1996 **Proceedings of the 33rd annual conference on Design automation**
Full text available: pdf(33.62 KB) Additional Information: full citation, references, citings, index terms

20 Piranha: a scalable architecture based on single-chip multiprocessing
Luiz André Barroso, Kourosh Gharachorloo, Robert McNamara, Andreas Nowatzyk, Shaz

Qadeer, Barton Sano, Scott Smith, Robert Stets, Ben Verghese
May 2000 **ACM SIGARCH Computer Architecture News , Proceedings of the 27th annual international symposium on Computer architecture**, Volume 28 Issue 2

Full text available: pdf(191.10 KB) Additional Information: full citation, abstract, references, citings, index terms

The microprocessor industry is currently struggling with higher development costs and longer design times that arise from exceedingly complex processors that are pushing the limits of instruction-level parallelism. Meanwhile, such designs are especially ill suited for important commercial applications, such as on-line transaction processing (OLTP), which suffer from large memory stall times and exhibit little instruction-level parallelism. Given that commercial applications constitute by fa ...

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